1. A method for synthesizing a clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said method comprising the steps of:

allocating at least one delaying circuit within each of said functional circuits;

fabricating an intra-functional clock distribution network within each of the functional circuits;

fabricating an inter-functional clock distribution network between each of the functional circuits;

determining a clock skew for the inter-functional clock distribution network; and

compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network.

2. The method of claim 1 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

3. The method of claim 2 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

4. The method of claim 3 wherein adjusting said delaying circuit comprises the step of connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.

5. An apparatus for synthesizing a clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said apparatus comprising:

means for allocating at least one delaying circuit within each of said functional circuits;

means for fabricating an intra-functional clock distribution network within each of the functional circuits;

means for fabricating an inter-functional clock distribution network between each of the functional circuits;

means for determining a clock skew for the inter-functional clock distribution network; and

means for compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network.

6. The apparatus of claim 5 wherein means for compensating for said clock skew of said inter-functional clock distribution network comprises:

means for determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

means for adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

7. The apparatus of claim 6 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

8. The apparatus of claim 7 wherein the means for adjusting said delaying circuit comprises means for connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.

9. An apparatus for synthesizing a clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said apparatus comprising means for executing the steps of:

allocating at least one delaying circuit within each of said functional circuits;

fabricating an intra-functional clock distribution network within each of the functional circuits;

fabricating an inter-functional clock distribution network between each of the functional circuits;

determining a clock skew for the inter-functional clock distribution network; and

compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network;.

10. The apparatus of claim 9 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

11. The apparatus of claim 10 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

12. The apparatus of claim 11 wherein adjusting said delaying circuit comprises the step of connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.

13. A clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said clock distribution circuit comprising:

at least one delaying circuit placed within each of said functional circuits;

an intra-functional clock distribution network within each of the functional circuits; and

an inter-functional clock distribution network between each of the functional circuits;

wherein a clock skew for the inter-functional clock distribution network is compensated by inserting said delaying circuit at a terminal of said

inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network.

14. The clock distribution circuit of claim 12 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

15. The clock distribution circuit of claim 14 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

16. The clock distribution circuit of claim 3 wherein adjusting said delaying circuit comprises the step of connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of the delaying

buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.

17. A integrated circuit synthesizing apparatus for synthesizing an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said integrated circuit synthesizing apparatus executing the steps of:

synthesizing a clock distribution circuit within said integrated circuit device, said synthesizing comprising the steps of:

allocating at least one delaying circuit within each of said functional circuits;

fabricating an intra-functional clock distribution network within each of the functional circuits;

fabricating an inter-functional clock distribution network between each of the functional circuits;

determining a clock skew for the inter-functional clock distribution network; and

compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network;.

18. The integrated circuit synthesizing apparatus of claim 17 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

19. The integrated circuit synthesizing apparatus of claim 18 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

20. The integrated circuit synthesizing apparatus of claim 19 wherein adjusting said delaying circuit comprises the step of connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of

the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.

21. A medium for retaining a computer program which, when executed on a computing system, executes a process for synthesizing a clock distribution circuit within an integrated circuit device, said device comprised of a plurality of functional circuits and placed on a substrate, said process comprising the steps of:

allocating at least one delaying circuit within each of said functional circuits;

fabricating an intra-functional clock distribution network within each of the functional circuits;

fabricating an inter-functional clock distribution network between each of the functional circuits;

determining a clock skew for the inter-functional clock distribution network; and

compensating for the clock of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-function clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network.

22. The medium of claim 20 wherein compensating for said clock skew of said inter-functional clock distribution network comprises the steps of:

determining a clock skew factor for one selected functional circuit connected to one selected terminal of said inter-functional clock distribution network; and

adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor.

23. The medium of claim 21 wherein said delaying circuit includes:

a plurality of delaying buffer circuits, each delaying buffer circuit having an first increment of delay; and

a plurality of interconnecting wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay.

24. The medium of claim 22 wherein adjusting said delaying circuit comprises the step of connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnecting wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor.